

What is claimed is:

1 1. An arithmetic operation method for a cyclic redundancy
2 check which performs arithmetic operations for error detection
3 on data to be transmitted using a plurality of generative polynomials
4 and is used in a communications system in which transmission of
5 said data is accomplished by adding a result from each of said
6 arithmetic operations to said data, said arithmetic operation method
7 comprising:

8 first arithmetic operation processing in which a first
9 arithmetic operation is performed on said data by a specified number
10 of bits using a first generative polynomial;

11 second arithmetic operation processing in which a second
12 arithmetic operation is performed on said data by a specified number
13 of bits using at least one piece of a second generative polynomial
14 being same as or different from said first generative polynomial;
15 and

16 third arithmetic operation processing in which a third
17 arithmetic operation is performed on said data of a specified number
18 of bits and on at least one piece of an arithmetic operation result
19 being obtained at a midpoint in either of said first arithmetic
20 operation or said second arithmetic operation, or in both said
21 first arithmetic operation and second arithmetic operation.

1 2. The arithmetic operation method for the cyclic
2 redundancy check according to Claim 1, wherein, in said third
3 arithmetic operation processing, said third arithmetic operation
4 is performed by handling said data of said specified number of
5 bits as low-order bits and by handling at least one piece of said

6 third arithmetic operation result as high-order bits.

1 3. An arithmetic operation method for a cyclic redundancy
2 check which performs arithmetic operations for error detection
3 on data to be transmitted using a plurality of generative polynomials
4 and is used in a communications system in which transmission of
5 said data is accomplished by adding a result from each of said
6 arithmetic operations to said data, said arithmetic operation method
7 comprising:

8 first arithmetic operation processing in which a first
9 arithmetic operation is performed on said data by 32 bits using
10 a thirty-second order generative polynomial;

11 second arithmetic operation processing in which a second
12 arithmetic operation is performed on said data by 32 bits using
13 a sixteenth order generative polynomial; and

14 third arithmetic operation processing in which a third
15 arithmetic operation is performed on said data of 32 bits and on
16 the first arithmetic operation result of 32 bits being obtained
17 at a midpoint in said first arithmetic operation processing using
18 said sixteenth order generative polynomial.

1 4. The arithmetic operation method for the cyclic
2 redundancy check according to Claim 3, wherein, in said third
3 arithmetic operation processing, said third arithmetic operation
4 is performed by 64 bits in total by handling said data of 32 bits
5 as low-order bits and said arithmetic operation result of 32 bits
6 as high-order bits.

1 5. An arithmetic operation method for a cyclic redundancy

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2 check which performs arithmetic operations for error detection
3 on data to be transmitted using a plurality of generative polynomials
4 and is used in a communications system in which transmission of
5 said data is accomplished by adding a result from each of said
6 arithmetic operations to said data, said arithmetic operation method
7 comprising:

8 first arithmetic operation processing in which a first
9 arithmetic operation is performed on said data by 32 bits using
10 a sixteenth order generative polynomial;

11 second arithmetic operation processing in which a second
12 arithmetic operation is performed on said data by 32 bits using
13 said sixteenth order generative polynomial;

14 third arithmetic operation processing in which a third
15 arithmetic operation is performed on said data of 32 bits and on
16 a first arithmetic operation result of 16 bits being obtained at
17 a midpoint in said first arithmetic operation processing using
18 said sixteenth order generative polynomial;

19 fourth arithmetic operation processing in which a fourth
20 arithmetic operation is performed on said data by 32 bits using
21 said sixteenth order generative polynomial; and

22 fifth arithmetic operation processing in which a fifth
23 arithmetic operation is performed on said data of 32 bits, said
24 first arithmetic operation result of 16 bits, and a second arithmetic
25 operation result of 16 bits being obtained at a midpoint in said
26 second arithmetic operation processing using said sixteenth
27 generative polynomial.

1 6. The arithmetic operation method for the cyclic
2 redundancy check according to Claim 5, wherein, in said third

7. An arithmetic operation circuit for a cyclic redundancy check which performs arithmetic operations for error detection on data to be transmitted using a plurality of generative polynomials and is used in a communications system in which transmission of said data is accomplished by adding a result from each of said arithmetic operations to said data, said arithmetic operation circuit comprising:

- a first arithmetic operation section to perform a first arithmetic operation on said data by a specified number of bits using a first generative polynomial;
- a second arithmetic operation section to perform a second arithmetic operation on said data by said specified number of bits using at least one piece of a second generative polynomial being same as or different from said first generative polynomial; and
- a third arithmetic operation section to perform a third arithmetic operation on said data of said specified number of bits and on at least one piece of an arithmetic operation result being obtained at a midpoint in either of said first arithmetic operation or said second arithmetic operation, or in both said first arithmetic

20 operation and said second arithmetic operation using at least one
21 piece of said second generative polynomial.

1 8. The arithmetic operation circuit for the cyclic
2 redundancy check according to Claim 7, further comprising a data
3 combining section to combine said data of said specified number
4 of bits handled as low-order bits with at least one piece of said
5 arithmetic operation result handled as high-order bits and to feed
6 combined results to said third arithmetic operation section.

1 9. An arithmetic operation circuit for a cyclic redundancy
2 check which performs arithmetic operations for error detection
3 on data to be transmitted using a plurality of generative polynomials
4 and is used in a communications system in which transmission of
5 said data is accomplished by adding a result from each of said
6 arithmetic operations to said data, said arithmetic operation
7 circuit comprising:

8 a first arithmetic operation section to perform a first
9 arithmetic operation on said data by 32 bits using a thirty-second
10 order generative polynomial;

11 a second arithmetic operation section to perform a second
12 arithmetic operation on said data by 32 bits using a sixteenth
13 order generative polynomial; and

14 a third arithmetic operation section to perform a third
15 arithmetic operation on said data of 32 bits and on an arithmetic
16 operation result of 32 bits being obtained at a midpoint in said
17 first arithmetic operation section using said sixteenth order
18 generative polynomial.

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1 10. The arithmetic operation circuit for the cyclic
2 redundancy check according to Claim 9, further comprising a data
3 combining section to combine said data of 32 bits handled as low-order
4 bits with said first arithmetic operation result of 32 bits handled
5 as high-order and to feed combined results to said third arithmetic
6 operation section.

1 11. An arithmetic operation circuit for a cyclic redundancy
2 check which performs arithmetic operations for error detection
3 on data to be transmitted using a plurality of generative polynomials
4 and is used in a communications system in which transmission of
5 said data is accomplished by adding a result from each of said
6 arithmetic operations to said data, said arithmetic operation
7 circuit comprising:

8 a first arithmetic operation section to perform a first
9 arithmetic operation on said data by 32 bits using a sixteenth
10 order generative polynomial;

11 a second arithmetic operation section to perform a second
12 arithmetic operation on said data by 32 bits using said sixteenth
13 order generative polynomial;

14 a third arithmetic operation section to perform a third
15 arithmetic operation on said data of 32 bits and on a first arithmetic
16 operation result of 16 bits being obtained at a midpoint in said
17 first arithmetic operation section using said sixteenth order
18 generative polynomial;

19 a fourth arithmetic operation section to perform a fourth
20 arithmetic operation on said data by 32 bits using said sixteenth
21 order generative polynomial; and

22 a fifth arithmetic operation section to perform a fifth

23 arithmetic operation on said data of 32 bits, said first arithmetic
24 operation result, and a second arithmetic operation result of 16
25 bits being obtained at a midpoint in said second arithmetic operation
26 section using said sixteenth order generative polynomial.

1 12. The arithmetic operation circuit for the cyclic
2 redundancy check according to Claim 11, further comprising:

3 a first data combining section to combine said data of 32
4 bits with said first arithmetic operation result and to feed a
5 combined result to said third arithmetic operation section, wherein
6 as said combined result, said data of 32 bits is placed at low-order
7 bits and said first arithmetic operation result is placed at
8 high-order bits, and

9 a second data combining section to combine together said
10 data of 32 bits, said first arithmetic operation result, and said
11 second arithmetic operation result and to feed a combined result
12 to said fifth arithmetic operation section, wherein as said combined
13 result said data of 32 bits is placed at low-order bits and said
14 first arithmetic operation result is placed at middle-order bits,
15 and said second arithmetic operation result is placed at high-order
16 bits.